Specifically, shared communication registers mapped into the address space of multiple processing elements may more quickly and more efficiently communicate data, such as graphics data, between the multiple processing elements. For instance, each of the communication registers may couple a first of the processing elements to every other processing element. Thus, faster and more efficient communication of data between the processing elements is provided as compared to sharing data between processing elements using separate registers between each pair of processing elements, and/or using registers having addressing that are not mapped into the addressing space of each processing element. For Example, ~~DETAILED DESCRIPTION~~ **Figure 1A** is a block diagram of a cluster of nine interconnected image signal processors...

Respectfully submitted,

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